IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR INC., Defendants.	Case No. 2:22-cv-293-JRG JURY TRIAL DEMANDED (Lead Case) [redacted]
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-cv-294-JRG JURY TRIAL DEMANDED

NETLIST, INC.'S SUR-REPLY IN OPPOSITION TO MICRON'S MOTION FOR SUMMARY JUDGMENT OF LACK OF WRITTEN DESCRIPTION FOR U.S. PATENT NO. 11,093,417 (DKT. 370)

I. A Reasonable Jury Could Find Written Description Support for the "CAS Latency" Limitation

The Court construed "overall CAS latency" as "the delay between (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module." Dkt. 228 at 36. Micron contends that the Court's construction "requires looking at when data is made available either (i) to a memory module from a host computer in response to a write command or (ii) from a memory module to a host computer in response to a read command." Reply at 2. In other words, under Micron's view, "the time when data is made available to or from the memory module" really means "the time when data is made available to or from the memory module*'s data pins, from or to the host computer*." But even under that interpretation, a reasonable jury could find that for write operations, there would be circumstances under which the overcall CAS latency of the memory module is greater than that of the actual operational CAS latency of each DRAM device. For instance, [redacted]

Thus, depending on the time difference between when the memory module receives/executes a write command and when the DRAM devices execute registered write command relative to the time difference between when the data reaches the DIMM data pins and when the data reaches the DRAM data pins, the last limitation could be satisfied in at least some circumstances even under Micron's interpretation. For instance, assume that the DIMM executes a write command at clock cycle 0, and write data reaches the module data pin 3 cycles later, then under Micron's interpretation, the overall latency would be three. In contrast, assume that (i) it takes one clock cycle for the module logic to process the received write command and forward the command to the DRAM devices, and (ii) there is a half-cycle delay in the data buffer, then under Micron's interpretation of operational CAS latency for DRAM—then the DRAM receives the write command at cycle 1 and data at cycle 3.5, making the

actual operational latency for the DRAM 2.5. The actual operational latency for the DRAM for the write operation would be even shorter (*e.g.*, 1.5 cycles) if there is additive latency, which delays when the write command is even released to the DRAM for execution. [redacted]; Ex. 7 (JESD79-2) at 24, § 2.2.4.1; Ex. 8 (IPR2023-01141 Petition) at 95 (Micron not including AL as part of CAS latency for DRAMs). In other words, a POSITA would recognize that even under Micron's interpretation, the last limitation would be met for write operations under some circumstances, and that would be sufficient for written description because the law does not require the condition be met at all times.

Moreover, Micron ignores the context of the claim language and the Court's statements emphasizing that the claims refer to "'data transfers *through* the circuitry,' '417 Patent at 42:63." Dkt 228 at 33. This supports Netlist's position that the time "when data is made available" to/from the memory module has to account for the additional delay caused by the circuitry. Micron's Reply does not meaningfully engage with the fact that the court's *Markman* order expressly relied on the specification in arriving at its construction of the "CAS latency limitation," showing that the term as construed by the Court has direct support in the specification. Indeed, the *Markman* order expressly states that "the last two limitations of Claim 1 of the '417 Patent concern CAS latency, '417 Patent at 42:54–67, ***which the patent discloses*** under the "Serial-Presence-Detect Device" section, *id.* at 22:36–62." Dkt. 228 at 20, n.8. [redacted] Micron cites *Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1319 (Fed. Cir. 2013), to argue that "a specification can help identify meaning of a claim term without providing adequate written description." Reply at 3. But *Trading Techs.* is not on point, because it does not involve a circumstance, as here, where a term was expressly construed to align with a portion of the specification. In contrast, in *Trading Techs.*, the Federal Circuit found the district court overly relied on a previous Federal Circuit decision construing claim terms in a related patent without properly

analyzing the scope and disclosures of the patents in question.

Micron spends the bulk of its analysis in reply selectively quoting the Court's construction and/or unfaithfully paraphrases the Court's construction to insert its own gloss. For example, Micron accuses Netlist of "changing the Court's construction of 'the time when data is ***made available to . . . the memory module***' to the 'time the data is ***available from the buffers*** to the memory devices'." Reply at 1 (ellipses and emphasis in original). Micron's omission of the words "or from" in the Court's construction is highly misleading. [redacted] Opp. at 5. In other words, the relevant endpoint in the Court's construction and the specification is considered from the perspective of the receiving DRAMs. Micron's motion cited the passage where Dr. Mangione-Smith opines as such (Mot. at 7), and its reply cites this passage in part (Reply at 2), but in both instances, Micron fails to meaningfully engage with Dr. Mangione-Smith's views.

Micron's two critiques of the disclosure identified by Dr. Mangione-Smith both fail. First, Micron states that the disclosure relates to a data buffer, i.e., "a discrete component that can be placed on a memory module," which Micron argues is contrary to the Court's construction, which it asserts "requires looking at the timing with respect to the 'memory module.'" Reply at 2. The problem with this critique is that a memory module is, by its very nature, a unit that combines multiple components, including (in the case of LRDIMM) a PCB, an RCD, and data buffers. A POSITA discussing timing with respect to the memory module as a whole is not limited to discussing timing with respect to the data pins on the PCB, as Micron argues. Micron's second critique is based on its interpretation that the Court's construction "requires looking at when data is made available either (i) to a memory module from a host computer in response to a write command or (ii) from a memory module to a

host computer in response to a read command." Reply at 2. As discussed above, even under that interpretation, there could still be situations where the last limitation is met for write operations.

Finally, Netlist pointed out that Micron did not move to strike Dr. Mangione-Smith's written description rebuttal analysis, which amounts to a concession of its reliability. Opp. at 6. In reply, Micron insinuates it did move to strike these opinions, which is simply false. *See* Reply at 5; Dkt 369.

II. A Reasonable Jury Could Find Written Description Support for "Data Buffer Control Signals" Prior to the '417 Patent Application

Micron states that "Netlist failed to substantively respond to [its] argument" that disclosure of "control signals" in earlier applications does not provide written description support for "data buffer control signals" because the 417 patent claims both "control signals" and "data buffer control signals." Reply at 4. In the specification, some of the control signals are used to control the operation of the memory devices, and some are used to control the operation of the switches/buffers. *See, e.g.*, '417, 7:32-37; 16:34-48. The claim differentiates the two types of control signals by referring to the ones for DRAMs as "control signals" and those for buffers as "data buffer control signals." But that does not mean a POSITA would not recognize that the inventors were in possession of both types of control signals at the time of the inventions. Micron cites no authority to the contrary. The only case Micron musters analyzes the claim construction principle of claim differentiation, and itself acknowledges that "[c]laims that are written in different words may ultimately cover substantially the same subject matter." *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005).[1]

Micron misstates the facts with respect to the '314 patent. Micron's motion sought summary judgment that there was no written description support prior to the 417 patent application. As Micron acknowledges, Netlist cited the abstract and lines 7:20-23 of the '314 patent as evidence of written description prior to the '417 application provided support. Micron now inappropriately tries to shift

[1] Micron's citation to a claim construction doctrine is notable given that earlier in its brief it argues that written description and claim construction are distinct inquiries. *See* Reply at 3.

the goalposts of the relief it is seeking. [redacted]

Micron's quibbling with Netlist's citation to the prosecution history merely highlights factual disputes that are live between the parties, rendering summary judgment inappropriate. For example, Micron asserts that "[t]he examiner was referring to the specification of the '417 patent only" when the examiner stated the "data buffer control signal" limitation was "taught in the specification as originally filed." Reply at 5. At best, this shows a fact in dispute. Even if the examiner did not cite specific support in his reasoning, the conclusion by the examiner (who evaluates validity from the perspective of a POSITA) is evidence of what a POSITA would have concluded based on the totality of the original disclosure.

Micron now disavows the arguments in its joint responsive claim construction brief with Samsung regarding "data buffer control signals" that acknowledged the disclosure in pre-417 portions of the specification. *See* Dkt. 143 (Defendant's CC brief) and 228 (CC order) at 29-30 (treating it as "defendants' construction" – not just Samsung's). Notably, Micron never stated in the responsive claim construction brief that it disagreed with that position or attributed that argument only to Samsung. Clearly, Micron wanted to have its cake and eat it too.

Micron mischaracterizes Netlist's position regarding Dr. Stone's arguments in his rebuttal report. [redacted] Micron also mischaracterizes Dr. Stone's

opinions in his opening report. Contrary to Micron's assertion, [redacted] First, Mr. Gillingham is a JEDEC expert, not a technical expert witness. Second, he was not shown any context regarding the '417 patent's disclosure, which makes clear that the FET switches are being used to buffer data signal lines. *See* '417, 9:46-52.

Finally, [redacted] *Contra* Reply at 6. Rather, he [redacted] concluded that the specification "describe[s the] invention . . . in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought." *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997).

III. Conclusion

For the foregoing reasons, the Court should deny Micron's motion for summary judgment.

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Respectfully submitted,

/s/ Jason Sheasby

Samuel F. Baxter
Texas State Bar No. 01938000
sbaxter@mckoolsmith.com
Jennifer L. Truelove
Texas State Bar No. 24012906
jtruelove@mckoolsmith.com
MCKOOL SMITH, P.C.
104 East Houston Street Suite 300
Marshall, TX 75670
Telephone: (903) 923-9000
Facsimile: (903) 923-9099

Jason Sheasby (*pro hac vice*)
jsheasby@irell.com
Annita Zhong, PhD (*pro hac vice*)

hzhong@irell.com
Thomas C. Werner (*pro hac vice*)
twerner@irell.com
Andrew Strabone (*pro hac vice*)
astrabone@irell.com
Yanan Zhao (*pro hac vice*)
yzhao@irell.com
Michael W. Tezyan (*pro hac vice*)
mtezyan@irell.com
IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
Tel. (310) 277-1010
Fax (310) 203-7199

Rebecca Carson (*pro hac vice*)
rcarson@irell.com
IRELL & MANELLA LLP
840 Newport Center Drive, Suite 400
Newport Beach, CA 92660

Attorneys for Plaintiff Netlist, Inc.

CERTIFICATE OF SERVICE

I hereby certify that, on February 15, 2024, a copy of the foregoing was served to all counsel of record.

/s/ Jason Sheasby
Jason Sheasby

CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL

I hereby certify that the foregoing document and exhibits attached hereto are authorized to be filed under seal pursuant to the Protective Order entered in this Case.

/s/ Jason Sheasby
Jason Sheasby